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AND, OR, and XNOR Optical Logic Gates via Pixel-Wise Modulation with Spatial Light Modulators and 4f System

Felipe Maia Prado
Center of Lasers and Applications
Nuclear and Energy Research Institute
São Paulo, Brazil
https://orcid.org/0000-0001-9350-2496

Sidney Leal da Silva
Optics and Applications Group
Fatec Itaquera
São Paulo, Brazil
https://orcid.org/0000-0001-7663-5545

Niklaus Ursus Wetter
Center of Lasers and Applications
Nuclear and Energy Research Institute
São Paulo, Brazil
https://orcid.org/0000-0002-9379-9530

***Abstract*—We present a simple optical setup based on two cascaded reflective phase-only spatial light modulators in a 4f configuration to perform basic logic operations in parallel. By adjusting polarization states and encoding binary input patterns as phase masks, we implemented three logic gates (AND, OR, and XNOR) with results consistent with the expected truth tables. The modulation relies on polarizing components to allow pixel-wise control across the entire image. Experimental results show good agreement with the target amplitude distributions and expected results.**

***Index Terms*—Optical computing, optical logic gates, spatial light modulator, polarization.**

I. Introduction

Optical computing has attracted attention in recent years due to its potential to accelerate linear operations, such as matrix multiplications, at high speeds and low energy cost, especially for applications in artificial intelligence [1]. Traditional computers, based on the von Neumann architecture, face limitations in bandwidth and efficiency when performing highly parallel tasks like neural network inference. Optical systems, on the other hand, offer massive parallelism, inherent low latency, and high bandwidth due to the nature of light propagation and multiplexing [1,2].

One foundational approach to optical computing relies on performing logic operations using devices such as Spatial Light Modulators (SLMs) or Digital Micromirror Devices (DMDs), which manipulate light by modulating its phase, polarization, or amplitude [3].

Previous works have explored various free-space optical setups for this purpose, including configurations based on Fourier optics and diffractive layers, demonstrating the potential for fully passive and reconfigurable logic systems [4]. Cascaded phase-only SLMs have also been shown to realize vector-matrix operations through polarization-based amplitude modulation [5].

Optical logic gates have long been proposed as fundamental building blocks for optical computing systems, leveraging the parallelism and high speed of light-based signal processing [6]. Various approaches using photonic circuits, diffractive optics, and free-space setups have been demonstrated to realize logic operations such as AND, OR, and XOR, with implementations ranging from integrated waveguide devices to spatial light modulators and diffractive neural networks [6,7]. While many of these configurations showcase advanced architectures or nonlinear elements, simpler, reconfigurable platforms based on optical modulators remain useful for prototyping and educational demonstrations of optical computing principles [8,9].

In this work, we demonstrate a simple experimental setup using two reflective phase-only SLMs in a 4f configuration to implement three basic logic gates (AND, OR, and XNOR) through polarization modulation. We present the behavior of each logic operation by sweeping pixel values and by applying 10×10 input grids, achieving effective amplitude modulation using only phase-only SLMs and linear polarizers.

II. Methodology

The optical setup begins with a wavelength-stabilized He–Ne laser emitting at 632.8 nm, with an output power of 20 mW, initially polarized in the vertical direction. The laser beam first passes through a spatial filter (SP) consisting of a microscope objective (10× magnification; NA = 0.25) and a 10 µm pinhole. After spatial filtering, the beam passes through a half-wave plate (WP1), which allows control over the polarization direction of the linearly polarized laser beam. The waveplate is followed by a collimating lens (L1) with a focal length of 300 mm.

The light is then directed to the first spatial light modulator (SLM1), which is a reflective, phase-only liquid crystal on silicon device with a resolution of 1920×1080 pixels (Model: Pluto, Manufacturer: HOLOEYE). The beam incident on SLM1 is diagonally polarized, adjusted by setting the WP1 at 22.5°.

The output of SLM1 is imaged onto SLM2 through a 4f system composed of two lenses (L2 and L3) with focal lengths $f_1 = f_2 = 150$ mm. Between the lenses of this imaging

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system, a linear polarizer is inserted to convert the phase modulation imparted by SLM1 into amplitude modulation.

SLM2 receives this modulated light, along with an additional polarization transformation introduced either by a linear polarizer (Pol.1) or a waveplate (WP2:$\lambda/2$ or $\lambda/4$) placed between SLM1 and SLM2. SLM2 displays a second image pattern and reflects the modulated light toward a CCD camera. This reflection is further relayed through a demagnifying telescope consisting of lenses L4 and L5 ($f_4 = 150$ mm and $f_5 = 75$ mm, respectively), which focuses the image onto the CCD sensor.

Before reaching the detector, the light passes through a final linear polarizer (Pol.2), converting the polarization-encoded modulation from SLM2 into amplitude variations. The resulting intensity is recorded at the CCD sensor plane. Figure 1, shows the general optical setup.

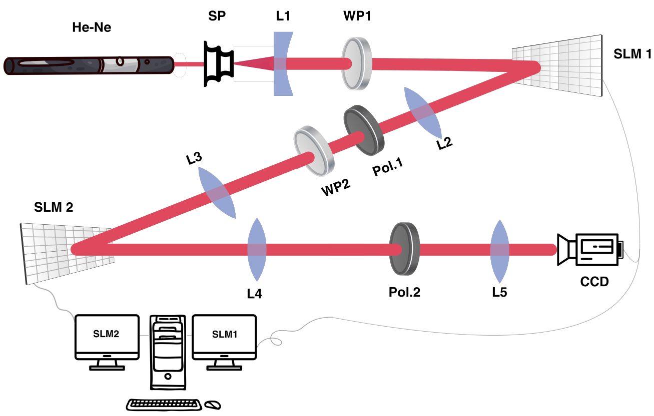

Fig. 1. Experimental setup for implementing optical logic gates. The setup consists of a He–Ne laser, followed by a spatial filter (SP), a collimating lens (L1), and a half-wave plate (HWP) to adjust the input polarization. The beam reflects off the first spatial light modulator (SLM1), and its output is directed through a 4f imaging system (L2 and L3) toward SLM2. A polarizer (Pol.1) between L2 and L3 converts the phase modulation from SLM1 into amplitude modulation. Additional polarization control (either by a waveplate or polarizer) can be placed between the SLMs depending on the logic operation. After SLM2, the beam passes through another lens (L4), a final polarizer (Pol.2), and is detected by a CCD camera.

The implementation of different logic gates (AND, OR, and XNOR) is achieved by modifying only the polarization elements between and after the SLMs. These specific configurations are detailed in the following subsections.

A. AND Optical Gate

To implement an AND logic operation, a polarizer set at $-45°$ is placed after SLM1 to remove the unmodulated component. This ensures that only light which has been phase-shifted by SLM1 (logical "1") propagates toward SLM2. After SLM2 applies its own phase mask, the beam passes through a final polarizer set at $+45°$. In this configuration, light reaches the detector only if both SLM1 and SLM2 modulate their respective regions, effectively implementing an optical AND gate.

B. OR Optical Gate

For the OR operation, a $\lambda/4$ waveplate oriented at $0°$ is placed between SLM1 and SLM2. This converts linear polarization into circular, allowing SLM2 to modulate a component orthogonal to the one affected by SLM1. A final polarizer at $-45°$ ensures that modulation by either SLM results in transmitted light. Thus, any input with at least one logical "1" leads to high intensity at the detector, corresponding to the OR truth table.

C. XNOR Optical Gate

The XNOR configuration uses a $\lambda/2$ waveplate set at $22.5°$ between SLM1 and SLM2 to rotate the polarization state such that both SLMs influence the same polarization axis. A final polarizer at $-45°$ ensures that the output intensity is high when both SLMs apply equal phases (both "0" or both "1"), and low otherwise. This corresponds to the logical XNOR operation.

III. Results and Discussion

To evaluate the optical logic gates implemented in our dual SLM setup, we experimentally measured the output intensity while varing the pixel values on one SLM and keeping the other fixed. This procedure was repeated for the configurations corresponding to the AND, OR, and XNOR logic operations. The normalized intensities recorded at the CCD sensor are shown in Fig. 2. For each case, black dots represent measure-

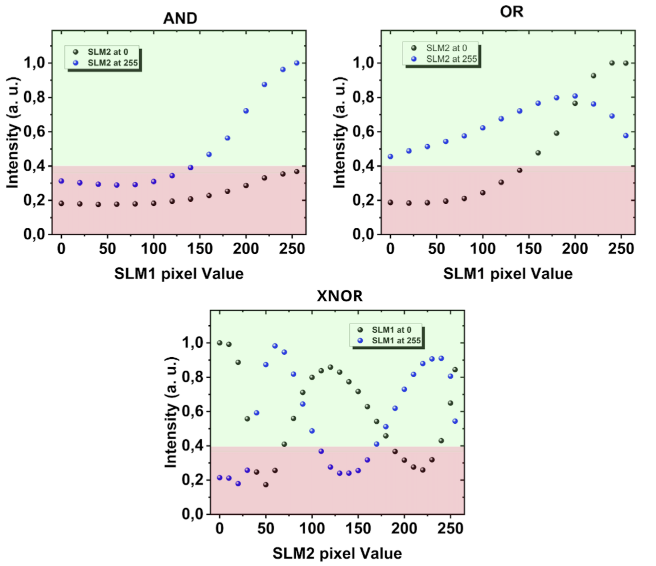

Fig. 2. Measured normalized intensities for optical logic gate operations. Top-Left: AND operation; Top-Right: OR operation; Bottom: XNOR operation. Each curve represents a sweep of pixel values for one SLM while the other is fixed at 0 (black) or 255 (blue). Red and green shaded areas represent logical "0" and "1", respectively.

ments when one SLM was fixed at pixel value 0, and blue dots when fixed at 255. The x-axis are the pixel values applied to the other SLM. The red and green shaded regions respectively indicate logical "0" and "1" output levels, based on an intensity threshold set to $I = 0.4$.

For the AND logic, significant intensity appears only when both SLMs apply high phase modulations (> 120 pixel value), verifying the expected “1” output.

In the OR logic configuration, high intensity is observed whenever either SLM modulates the beam. The blue curve always stays above the threshold since the pixel value is constantly high. When SLM2 is at 0, the output becomes high starting at the > 125 pixel value condition.

The optical XNOR logic curve presents high values whenever the logic values of both SLMs are the same (excluding pixel values > 240), and low values whenever the logic values of the two SLMs differ. Following the data acquired from Fig. 2, maximum modulation occurred with pixel values of 20 (logic value “0”) and 222 (logic value “1”). Values outside of these presented worse contrast or even unexpected results. This explains the error in the XNOR-like behavior of points above 230 in the XNOR graph. This behavior can be corrected via better calibration of the SLMs (bit value to the corresponding phase change).

In addition to these pixel-wise operations, logic operations were performed using grids (4x4 and 10x10) of binary input projected onto both SLM1 and SLM2. Figure 3 shows the input grids, as well as the normalized grids reflected by each SLM, and the expected and normalized experimental results for AND, OR, and XNOR gates.

The 4×4 inputs are complementary (SLM2 = ¬ SLM1), and are used to stress-test uniformity and gate polarity. For such inputs the outputs are uniform (AND = 0, OR = 1, XNOR = 0). The 10×10 masks include all input pairs.

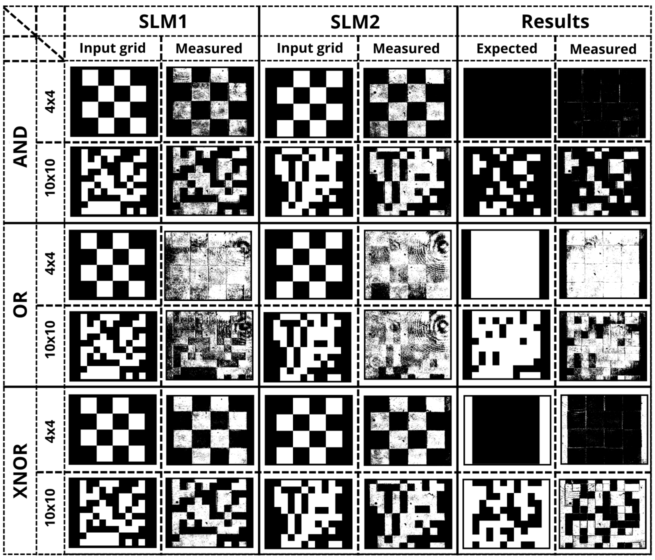

Fig. 3. Optical logic operations. Each logic gate (AND, OR, XNOR) was tested using 4×4 and 10×10 binary masks applied to both SLM1 and SLM2. Columns from left to right: SLM1 input, SLM1 measured output, SLM2 input, SLM2 measured output, expected result, and measured final result.

Each row of the figure corresponds to a specific logic operation and input resolution. From left to right, the columns represent: the input grid displayed on SLM1; the measured intensity at SLM1; the input grid displayed on SLM2; the measured intensity at SLM2; the expected binary output from the corresponding logical operation; and the final intensity pattern recorded at the CCD after the full optical path.

The results confirm that the implemented polarization-modulation scheme successfully performs pixel-wise logic operations in parallel. Although some noise and background modulation artifacts are observed, particularly in the 10×10 patterns and in the OR operation due to imperfections in the quarter-wave plate. The output images maintain strong structural agreement with the expected logical results, contributing the system’s spatial computing capability.

IV. Conclusion

In this work, we demonstrated the implementation of basic logic operations (AND, OR, and XNOR) using two cascaded SLMs. By adjusting the input and output polarization states and employing phase-only spatial light modulators, we were able to achieve pixel-wise logical behavior consistent with the expected truth tables.

The results showed good similarity with the expected amplitude modulation and successfully performed the desired logic operations in parallel. Limitations such as background modulation artifacts and noise were observed. Additionally, phase calibration remains critical, as the SLMs in this configuration do not provide full 2π modulation and exhibited nonlinear phase responses.

Future work can focus on calibration to improve the curves presented in Fig. 2, especially in the case of the XNOR gate, and extending to larger and more complex input patterns.

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